Design Guide for DP8473 in a PC-AT

National Semiconductor
Application Note 631
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December 1989

OVERVIEW

When designing a floppy interface circuit for a PC-AT in the past, there was very little flexibility given to the design engineer. The NEC765, which was designed into the original IBM PC, was the only floppy controller available that would guarantee compatibility. Compatibility is extremely important in a PC design.

There were many design issues that had to be resolved when using the NEC765 to produce a fully functional floppy controller interface. A data separator had to be selected or designed. A write precompensation circuit needed to be included. A whole score of miscellaneous logic had to be designed to handle all of the unique PC functions that the NEC765 does not handle itself.

The DP8473 from National Semiconductor was developed to eliminate all of these design problems. All of the extra functions and logic normally required for an XT or an AT design are included inside the chip. Even an analog data separator, which is classically the hardest function to design, has been integrated into the DP8473.

Compatibility has been completely retained. The DP8473 is software compatible with the NEC765A. We have not found any current software available for the PC that fails to work properly with the DP8473. This includes software running under DOS and OS/2.

This application note will discuss some of the issues involved in a floppy controller design with the DP8473. Even though on the surface, there may not seem to be many options when designing a floppy controller for a PC, there really are quite a few. Some of these options include: signal swapping in the floppy cable, different types of floppy drives, and data separator filter selection.

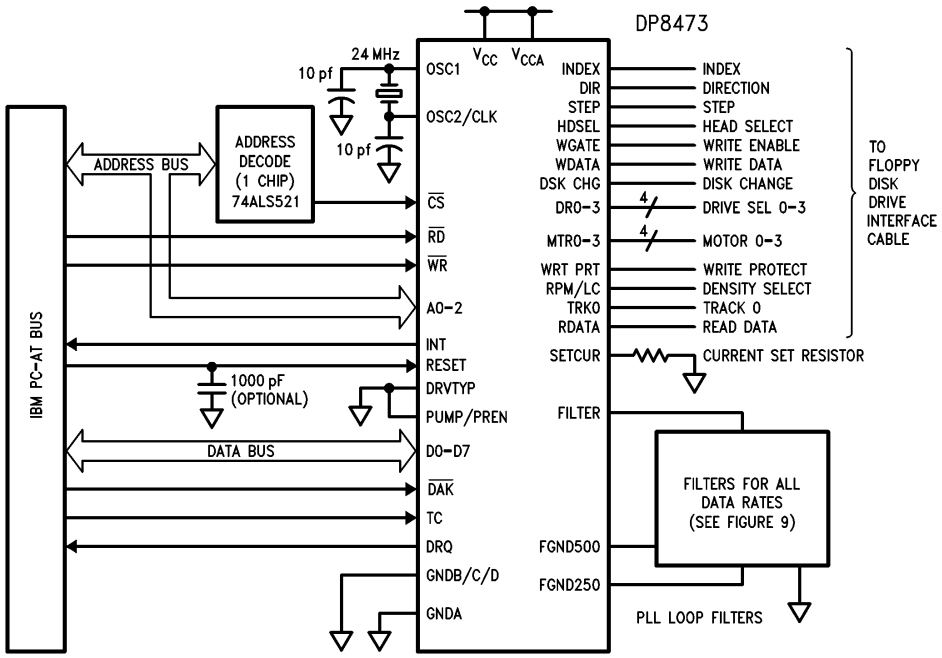

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FIGURE 1. Schematic of Typical DP8473 Floppy Controller Design

RRD-B30M75/Printed in U. S. A.

HARDWARE ENVIRONMENT

A typical floppy controller design with the DP8473 will look something like the schematic shown in *Figure 1*. You may be surprised that the entire schematic for the floppy controller design fits on less than one page. Especially if you consider that the schematic for a similar function in the IBM PC-XT technical reference manual takes four full pages.

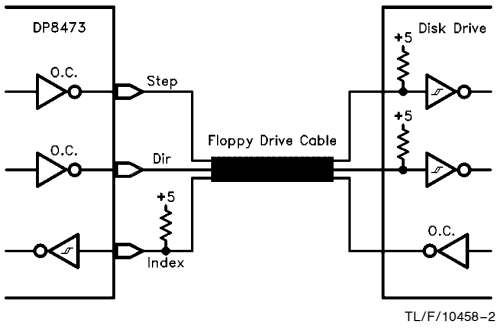
The heart of the design is, of course, the DP8473. Most of the interface pins to and from the DP8473 go directly to the peripheral bus or the disk drive cable without additional logic or buffering.

DRIVE CABLE INTERFACE

The DP8473 disk interface signals connect directly to the drive cable. Most disk drives terminate the drive cable with resistors. Termination is required because the output buffers of the floppy controller are open-collector.

Terminated signals are used because historically, relatively long cables have been used to connect the floppy controller to the disk drives. The cable termination will decrease the amount of crosstalk and noise on the drive cable signals.

A typical disk interface circuit consists of an open-collector output buffer at the signal source, and a termination resistor and a Schmitt input buffer at the signal destination. For example, the STEP output pin on the DP8473 is an open-collector output buffer that is capable of sinking up to 48 mA (See Note 1). If the output is off, the buffer is disabled, and the termination resistor on the disk drive will pull the signal high. If the STEP output is on, the DP8473 buffer will pull the signal low. An example of the cable termination logic is shown in *Figure 2*.



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Note 1: The DP8473 actually contains open-drain output buffers due to its CMOS design. The end result is the same as TTL open-collector buffers.

FIGURE 2. Example of Buffers and Terminators Used for Floppy Drive Interface

The termination resistors used with 5.25″ drives or 8″ drives typically have a value of 150Ω. With this resistor value, the output buffers must be capable of sinking about 35 mA each in order to pull the drive signal to a logic low level. The DP8473 is able to sink this current without external buffers.

The termination resistors used with 3.5″ drives are often 1 kΩ. 1 kΩ termination resistors are also sometimes found on low power 5.25″ drives. The larger termination values, which correspond to reduced drive buffering requirements, are due to a couple of factors. Drive manufacturers have recognized that the floppy interface cable used in a PC is relatively short. Also, the drives are installed in the same grounded enclosure as the PC and the floppy controller. This reduces the amount of noise introduced on the floppy interface cable.

If both 3.5″ drives and 5.25″ drives are to be used in an application, the termination resistors used with the DP8473 must be chosen carefully. The termination resistor value used with the DP8473 must be the larger of the termination resistors used on the drives. For example, if the 5.25″ drive has 150Ω termination resistors and the 3.5″ drive has 1 kΩ termination resistors, the termination resistors used on the inputs to the DP8473 should be 1 kΩ.

The termination resistors for the inputs to the DP8473 should be placed near the DP8473. The termination resistors for the outputs for the DP8473 to the disk drive are contained in the disk drive itself.

Additional disk interface buffering is not normally required when using the DP8473. It can sink up to 48 mA for each disk output signal. This is more than enough capacity for a typical floppy design.

DRIVE CONFIGURATION

A PC-XT can typically interface to up to four disk drives. A PC-AT, however, is usually limited to two disk drives. The two drive limitation is due to the ROM BIOS used in most AT's. More than two drives can be used if special software drivers are written.

The connection between the floppy drives and the floppy controller in a PC is slightly different than the SA450 standard used in non-PC's. The advantage to the method used in a PC is that each disk drive installed in the PC can be configured identically. Even the Drive Select strap is the same. Each drive is configured as drive 1 (or B). Even if four drives are all connected, they are each strapped as drive 1.

The trick used to accomplish this feat is cable wire swapping, where the drive and motor select signals are physically reversed on the floppy interface cable. The cable swapping re-routes the four DRIVE select signals (DR0, DR1, DR2, DR3) to the DR1 signal of each individual drive. For example, DR0 is routed to drive A's DR1 input. DR1 is routed to Drive B's DR1 input, and so on. In a similar manner, the cable swapping also re-routes the four MOTOR signals (MTR0, MTR1, MTR2, MTR3) to the MOTOR signal of each drive. *Figure 3a* demonstrates how the cable is configured for two floppy disk drives. A second cable would be used if more than two drives are required as shown in *Figure 3b*.

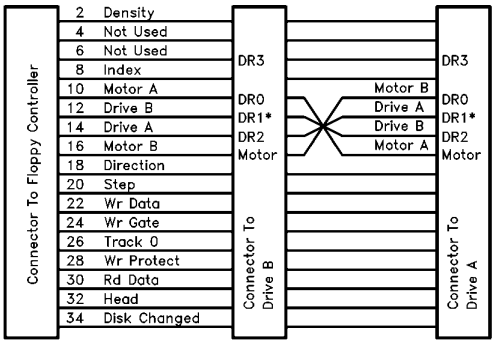

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FIGURE 3a. Cable Swapping Used for Drives A and B

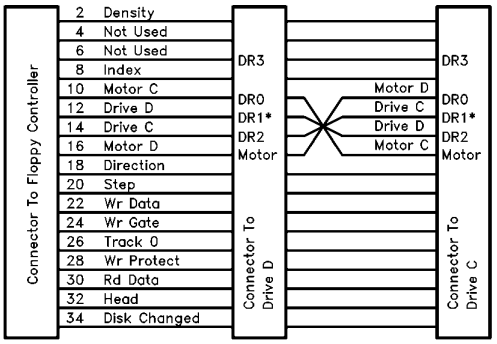

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FIGURE 3b. Cable Swapping Used for Drives C and D

Note: The asterisk (*) next to DR1 indicates that this drive is strapped as Drive 1. In the PC, all drives are strapped as Drive 1.

If more than one disk drive is attached to the floppy controller, there may be more than one drive terminated. This may cause a current overloading problem. The controller may not be able to drive an active signal low.

It is easy to prevent current overloading in a two disk drive PC. Simply make sure that only one drive is terminated. Ideally the terminated drive should be the drive at the end of the drive cable, although it could be either drive.

If both drives are terminated, the output buffers will be driving too much current. The system will be out of specification. This is a common situation and is largely ignored by PC manufacturers. The output buffers can usually handle the additional load.

It three or four drives are to be used, things become more complex. For example, if four 150Ω terminated drives are all attached to the DP8473, the DP8473 will have to sink 139 mA for each drive interface signal. The DP8473 is guaranteed to sink up to 48 mA. Therefore, this configuration would not work without additional buffering. Please refer to the sidebar, ''How to Calculate the Maximum Current Required for Output Buffers'', for a description on current calculation.

There are three techniques that can be used to prevent overloading the output buffers:

Technique 1:

Using larger termination resistors can reduce the load on the DP8473 to acceptable levels. Suppose 1 kΩ resistors can be used instead of 150Ω resistors. In the worst case where all four disk drives are terminated, only 21 mA will be generated instead of 140 mA. This is well within the specification of the DP8473. The 1 kΩ termination resistors are commonly used with 3.5″ drives.

Technique 2:

The most direct technique that can be used is simply adding additional buffers for the extra disk drives. Drives A and B can be driven directly by the DP8473. The outputs to drives C and D can pass through an open-collector buffer such as the 7407. This is shown in *Figure 4*. 1k pullup resistors are required for some of the DP8473 outputs because they are not terminated by drives A or B.

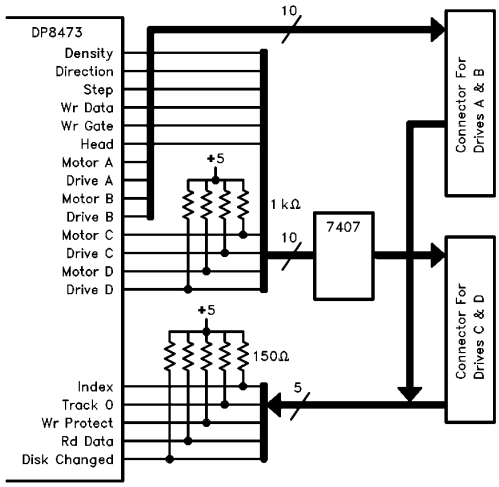

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FIGURE 4. Extra Buffers Required for Four Drive System

Technique 3:

Daisy chain the floppy drives with the controller on one end of the drive interface cable, and one terminated drive at the other end. One to three additional non-terminated drives can be added in the middle as shown in *Figure 6*. With this technique, the four Motor signals from the DP8473 should be wire-ORed together as shown in *Figure 5*. Each drive must be strapped for the proper drive select (0–3).

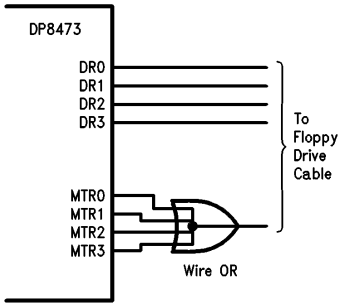

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FIGURE 5. Wire OR Required for Daisy Chain Connection

How to Calculate the Maximum Current Required for Output Buffers.

Since a floppy controller design may not work correctly due to current overloading, it is important to understand exactly how to calculate the maximum current required by the floppy controller for each output signal to the disk drive. This is largely determined by the termination resistors used by the disk drives. A formula that can be used is:

$$\frac{(V_{CC}) + (\text{Max } V_{CC} \text{ Variation}) - (V_{OL(max)})}{(\text{Termination Resistor}) \bullet \frac{1}{N} \bullet (1 - \text{Resistor Accuracy})}$$

$V_{CC} = 5.0$

Max V_{CC} Variation = Power supply variation (0.5V)

$V_{OL(Max)}$ = Maximum active low output voltage of buffer (0.8V)

Termination Resistor = Termination on disk drive

N = Number of terminated disk drives

Resistor Accuracy = Accuracy of termination resistors (10% or 0.10)

Example 1:

One terminated drive with 150 termination resistors.

$$\frac{5.0 + 0.5 - 0.8}{150 \bullet 1 \bullet 0.9} = 34.8 \text{ mA}$$

Example 2:

Four terminated drives with 1k termination resistors.

$$\frac{5.0 + 0.5 - 0.8}{1000 \bullet \frac{1}{4} \bullet 0.9} = 20.9 \text{ mA}$$

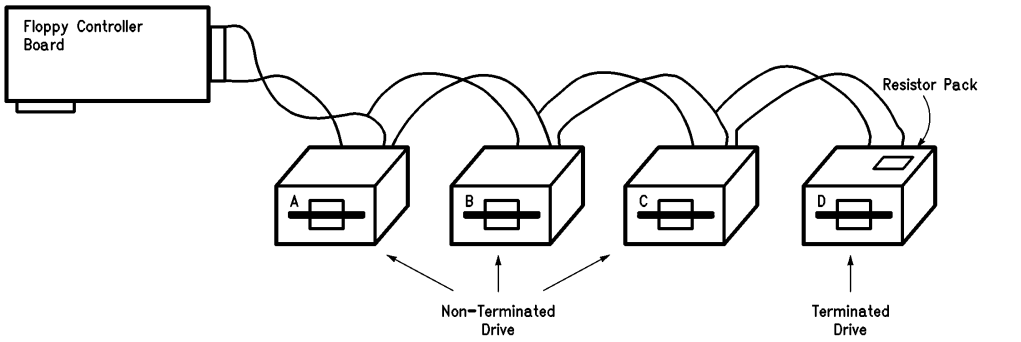

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FIGURE 6. Daisy Chain of Four Drives

DRIVE TYPES

There are many types of disk drives that can be connected to the DP8473 floppy disk controller. The DP8473 is compatible with 8″, 5.25″, and 3.5″ floppy disk drives, although 8″ drives are rarely used today.

Other types of peripherals may be connected to the floppy controller as well. A streaming tape drive that is used to back up the hard disk is often connected to the floppy controller. A tape drive of this type is very specialized. It has been designed to look like a floppy disk drive from an electrical interface point of view. It does not perform exactly like a disk drive, however. Special software is usually required to make it work correctly. The STEP signal is often used to issue commands to the tape drive. For example, to rewind the tape, four step pulses may need to be issued. To start a read, six step pulses might be issued.

All of these different drive types have one thing in common, a similar electrical interface. This allows them all to be connected to a common drive interface cable. For example, the READ DATA signal on pin 30 of the floppy interface cable is the MFM encoded serial stream of data from the disk. The INDEX signal on pin 8 of the cable identifies the beginning of a track.

However, there are some minor differences between drive tapes that must be considered. The DENSITY signal is a good example. This signal is active for *high* density transfers on a dual density 3.5″ drive. But, this signal is active for *low* density transfers on a dual density 5.25″ drive. This difference makes the floppy system design more complex when 5.25″ dual density and 3.5″ dual density drives are both used in the same PC.

The DP8473 has a signal called RPM/LC that normally connects to the Density or Low Current input on a dual density 5.25″ drive. If a 3.5″ drive is used, the RPM/LC output should be inverted.

A design such as the one shown in *Figure 7* could be used to create the proper DENSITY signal for both 5.25″ and 3.5″ drives. The jumpers and logic allow the user to select between drive types (5.25″ or 3.5″) for each individual drive.

Another solution is simply to use a 3.5″ drive that contains a built-in jumper to vary the polarity of the DENSITY signal directly on the drive. This option eliminates the need for external logic and jumpers.

Another signal that is drive type dependent is DISK CHANGED. This signal exists on low and dual density 3.5″ drives and also on dual density 5.25″ drives. It does not exist on low density 5.25″ drives. If a low density 5.25″ drive is to be used, the DISK CHANGED signal should be held active (low level). It may be held active by the drive by itself. If not, a pull-down resistor could be used to activate the non-driven signal.

One thing to consider while choosing drive types is media compatibility. Of course, you can't put a 3.5″ disk in a 5.25″ drive. But, there are more subtle incompatibilities even within similar media types. For example, a low density 5.25″ disk written to in low density mode by a dual density drive cannot be read reliably by a low density drive. Table I lists the compatabilities between different drives and media types.

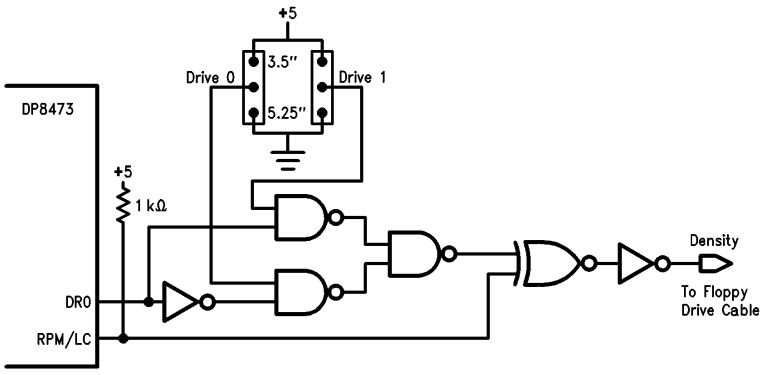

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FIGURE 7. Density Select Logic for 5.25″ or 3.5″ Drives

TABLE I. Drive and Media Compatibility

Drive Type	Mode	Media Type			
		3.5″	3.5″ HD	5.25″ DD	5.25″ HD
3.5″ LD	720k	R/W			
3.5″ LD,HD	720k 1.44M	R/W	R/W		
5.25″ LD	360k			R/W	
5.25″ LD,HD	360k 1.2M			R Only	R/W

Notes:

LD = Low Density
HD = High Density
R/W = Readable & Writable
R Only = Readable Only

DATA RATES

Different drive types may use different data rates. The data rate is specified by the number of bits that are transferred in a second. For example, 250 kb/s is translated to 250 thousand bits per second.

The data rate used by a disk drive is determined by the electronics of the drive and the specifications of the media. Low Density media require data to be transferred at 250 kb/s. High Density media is twice as fast at 500 kb/s.

There is a complication with Low Density 5.25″ media in a Dual Density drive. The 1.2 Mbyte drive spins the disk faster (360 RPM) than a 360 Kbyte drive (300 RPM). When a Low Density disk is read from a Dual Density drive, the data rate will be 300 kb/s instead of 250 kb/s because of the rotational speed difference.

The DP8473 can operate at all the data rates required for a PC. This includes 250, 300, and 500 kb/s. In addition, the DP8473 can operate at 1 Mb/s. This high data rate is starting to appear in both floppy disks and streaming tape drives.

μP INTERFACE

It is hard to imagine how the interface between the DP8473 and the μP bus could be made any simpler than it is. Only one interface function is not integrated in the DP8473. That function is address decoding. The typical μP connections are shown in *Figure 8*.

The DP8473 requires a CS (chip select) enable signal that could be generated by an ALS521 8-bit comparator or a similar circuit. Address decoding of the three least significant bits of the address is performed by the DP8473. The AEN (address enable) signal from the μP bus should be included in the CS decode logic. This will prevent DMA transfers from generating a CS.

The eight bit data bus from the DP8473 connects directly to the data bus of the μP. Bus transceivers are not required because 12 mA buffers are built into the DP8473.

The IOR (I/O read), IOW (I/O write), RESET, TC (terminal count), DRQ (DMA request), and IRQ (interrupt request) signals can be connected directly to the DP8473. No additional buffering or gating is required. The logic required to TRI-STATE® the DRQ and INT pins is integrated in the DP8473.

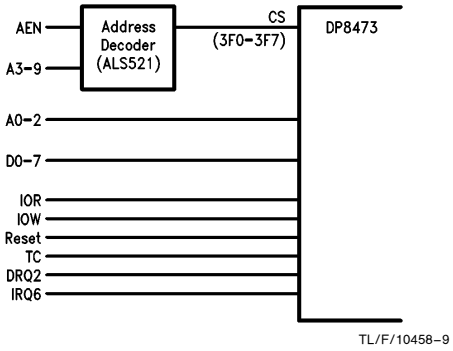

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FIGURE 8. μP Interface to DP8473

FILTER SELECTION

The internal data separator in the DP8473 requires an external filter to operate correctly. This filter is part of an analog Phase-Locked Loop (PLL) that is used by the data separator integrated into the DP8473. This is commonly referred to as an analog data separator due to the analog nature of the PLL's filter and Voltage Controlled Oscillator (VCO).

As the floppy controller changes from one data rate to another, the filter used by the PLL must change also. This is done automatically in the DP8473. Two or three filters are connected externally to different pins of the DP8473. The correct filter is selected and activated by the DP8473 itself.

The filter selection is performed by grounding or forcing TRI-STATE the appropriate filters. For example, a two-filter arrangement is shown in *Figure 9*. If 500 kb/s is selected, the FGND500 pin is grounded and the FGND250 pin is at TRI-STATE. From the filter pin's point of view, this appears as filter F2 in parallel with capacitor C1. F1 is electrically out of the picture. When 250 kb/s is selected, it is the opposite. The FGND500 pin is at TRI-STATE and the FGND250 pin is grounded. Since 300 kb/s data rate is close to 250 kb/s, the same filter is used for both data rates.

The two-filter arrangement shown in *Figure 9* would be used in most PC applications. It supports 250, 300, and 500 kb/s data rate. Other filter combinations may be used for specialized applications. These filter combinations are described in the DP8473 data sheet.

DATA SEPARATOR PERFORMANCE

One of the most important features of the DP8473 is the high level of data separator performance. This performance translates directly to reduced disk I/O errors. There is quite a bit of information that can be discussed on data separator performance. A lot of this information is presented in an application note titled ''Floppy Disk Data Separator Design Guide for the DP8473, AN-505''.

It might seem desirable to specify the maximum error rate of the DP8473. This could be expressed in terms of the number of bits that can be read correctly before an error occurs (10^{12}, for example). This is not a practical parameter to specify, however. One problem is the amount of time this type of measurement would take. A test of 10^{12} could take well over 400 days to measure.

Another problem is defining the test conditions. Is the test performed under ideal disk conditions? Are bits jittered or is motor speed variation simulated? There are so many variables in this type of a test that it would be difficult for two different people to produce the same results. In addition, the error rate is related to other factors beside the DP8473 such as the disk drive or the floppy media.

There are many different types of measurements that can be made with a data separator. Most of these measurements indicate how well only one particular section of the data separator performs. For example, the gain of the VCO (Voltage Controlled Oscillator) or the accuracy of the ¼ period delay line. They don't, however, give a good indication of how well the data separator will perform under real-life conditions.

There is one measurement that produces meaningful data. This measurement is called ''Dynamic Window Margin''. Dynamic window margin attempts to indicate total data separator performance under real-life conditions. It measures how much bit jitter the data separator can handle while reading a worst case data pattern (DB6 hex) with a drive that has a motor speed of varying accuracy. The data is jittered in a manner similar to real world jitter with a reverse write precompensation pattern. The measurement is taken at the worst point over a motor speed variation of ±6%. An example of a dynamic window margin measurement is shown in *Figure 10*.

The typical dynamic window margin is specified in the DP8473 data sheet. National Semiconductor has made measurements of the dynamic window margin of many data separators, and the results show that the DP8473 data separator's performance is very competitive.

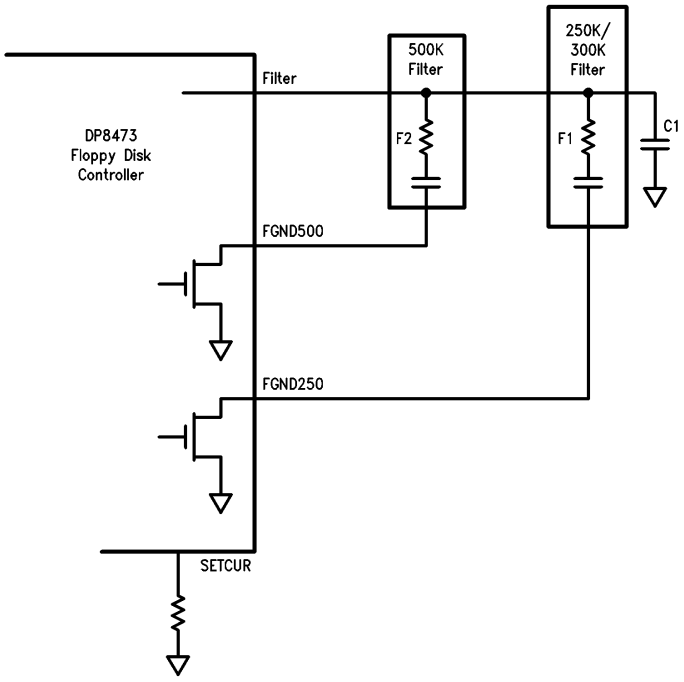

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FIGURE 9. Typical Filter Connection for 250, 300, and 500 kb/s

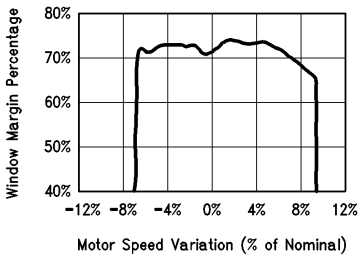

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FIGURE 10. Typical Dynamic Window Margin for DP8473

LAYOUT AND COMPONENT CONSIDERATIONS

The DP8473 contains a combination of digital and analog circuitry. Because of the analog nature of the data separator, some precautions should be taken when designing a board with the DP8473.

A good DP8473 board layout design will distinguish between the analog and digital power supply pins, namely V_{CC} and Ground. The supply pins used by the digital circuitry are labeled V_{CC}, GNDB, GNDC, and GNDD. The supply pins used for the analog data separator are labeled V_{CC}A and GNDA. Standard digital decoupling techniques should be used with the digital supply pins. This typically involves 0.1 μF capacitors connected between V_{CC} and GND.

The analog supply pins require a bit more consideration than the digital supply pins. Any noise or ripple on the analog supplies will degrade the data separator performance. It is recommended to minimize this noise as much as possible. Less than 50 mV noise would be good.

There are many methods that can be used to minimize noise on the analog supply pins. One of the best methods is a 5.0V voltage regulator dedicated to the analog section. This guarantees a very clean signal. The voltage regulator can be driven by the +12V supply pin on the AT bus.

Another method is to place the DP8473 on the board close to the entry point of the power supply. At the very least, separate supply lines should be dedicated from the power supply entry point on the board to the DP8473 V_{CC}A and GNDA.

In addition to the analog supply, any noise or crosstalk introduced to the external filters will adversely effect the performance of the data separator. The data separator filters should be positioned as close as possible to the DP8473. A ground plane surrounding the filters would also be advisable. The resistor attached to the SETCUR pin should also be close to the DP8473.

If a 24 MHz crystal is used, it should be placed close to the DP8473 as well as the 10 pF capacitor attached to both sides of the crystal.

The component types and tolerances may also effect the data separator performance. The accuracy of the resistor attached to the SETCUR pin is important. It should have a 1% tolerance rating. A 5% could be used, but the accuracy may effect the data separator performance.

The capacitor in series with the resistor attached to the FILTER pin is also critical. It should have a 5% tolerance. The series resistor in the same network is not as critical as the SETCUR resistor. Therefore, a normal 5% tolerance can be used here.

Finally, the capacitor in parallel with the filter network can be rated as low as 10%–20%. It does not effect the data separator very much.

The component tolerances mentioned here are only recommendations. The DP8473 will work properly with a wide range of filter values. These recommendations should be followed if data separator performance is an important issue in a particular design (which is normally true).

TROUBLE-SHOOTING

If the floppy controller does not appear to operate correctly, there are some key areas that can be looked at for the source of the problem.

The disk drive's in Use light remains on at all times.

- Drive Interface cable plugged in backward.
- Drive Interface signals not properly routed.

DOS returns a ''Not ready error reading drive X''.

This error can be caused by many different problems. At this point it would be best to run the ''Floppy Demo Program'' as described later in this section.

DOS Directory command returns an old directory.

- Disk Changed signal improperly routed on drive interface cable.

POST produces a ''601'' error while booting.

- Drive Interface cable unplugged.
- Hardware problem with μP interface.

PC locks up while booting.

- Hardware problem with μP interface.

Parity Error.

- DMA interface problem.

Many advanced diagnostics may be used while running the ''Floppy Demo Program'' which is available from National Semiconductor. This program allows you to issue individual floppy commands such as Read Data, Format Track, and Seek. The Result Phase of these commands can be analyzed to help determine where a problem exists. The following list describes some likely sources of problems based on what is observed with the ''Floppy Demo Program''.

''Missing Address Mark in Address Field'' error.

This indicates that the floppy controller could not find any valid data on the track being read. No sectors could be found.

- Track has not been formatted. Could be a blank disk. The controller does recognize Index Pulses, however. This indicates that the drive cable interface is at least partially intact.
- Read Data drive interface signal not properly routed.
- General data separator problem. See the data separator discussion later.

''Did not receive interrupt'' error.

This is usually accompanied with all FF's in the Result Phase of the command. This indicates that the controller could not read anything from the disk drive and Index pulses were not seen. Be sure to reset the floppy controller after this error.

- Disk not inserted in drive or drive door open.
- Wrong drive selected in command.
- Drive Interface cable unplugged.

MSR (Main Status Register) does not return to 80 (hex) after a reset.

- Floppy controller not inserted in socket properly.
- Hardware problem with address decode (CS) or μP interface signals.
- Crystal or external clock not operating properly.
- Floppy controller is bad.

"No Data" error or "CRC error".

- Bad disk media.
- General data separator problem.

Fewer bytes read than requested or error in Result Phase.

- Noise on Reset pin. Insert capacitor between Reset and digital GND as specified in the data sheet.

Long term read produces some errors.

- General data separator problem.

Many of the problems described above refer to a general data separator problem. There are many things that can be looked at for data separator problems.

- Filter wired incorrectly.
- Incorrect filter component values.
- Filter layed-out poorly.
- Too much noise on analog $V_{CC}A$ or GNDA.

FLOPPY CONTROLLER DESIGN WITH NEC765A

In order to appreciate the amount of circuitry integrated into the DP8473, it may be useful to analyze a typical floppy controller design for the PC-AT using the standard NEC765A floppy disk controller. To simplify the analysis, only the block diagram will be presented. The actual schematic would require many pages. The block diagram is shown in *Figure 11*.

The NEC765A was developed many years ago originally for 8″ floppy disk drives. It became very popular because it was designed into the original IBM PC. The NEC765A performs many functions, but there are also many functions that it does not perform.

A data separator isolates the individual pulses read from the disk drive and allows the floppy controller to distinguish between MFM clock pulses and data pulses. It typically incorporates an analog PLL. An analog data separator design could require as many as 10 chips to design. A single chip discrete digital data separator could also be used, although the performance will be poor.

The write precompensation circuit shifts the MFM encoded data as it is being written to the disk. This shifting compensates for known bit shifts that will occur due to the magnetic influences of the individual bits recorded on the disk. This is typically designed with a shift register and a multiplexer.

The NEC765 cannot interface directly to the Drive Interface cable. Separate 48 mA buffers are required for each output signal. This requires three 7406's. Also, the inputs from the disk drive require Schmitt inverters.

Additional buffering is also required for the μP data bus. This would be done with an LS245 octal bus transceiver.

The PC-AT requires that the Disk Changed signal be read from a particular port. This involves address decoding and buffering.

The only method available to vary the data rate used by the NEC765A is by altering the input clock frequency to the chip. This must be done with a complex divider circuit that generates the different frequencies required for 250, 300, and 500 kb/s data rates.

Due to timing incompatibilities in the NEC765A, the Drive Select and Motor On signals must be generated by an external port that is controlled by software. This port also controls the software reset and DMA and INT enable circuitry.

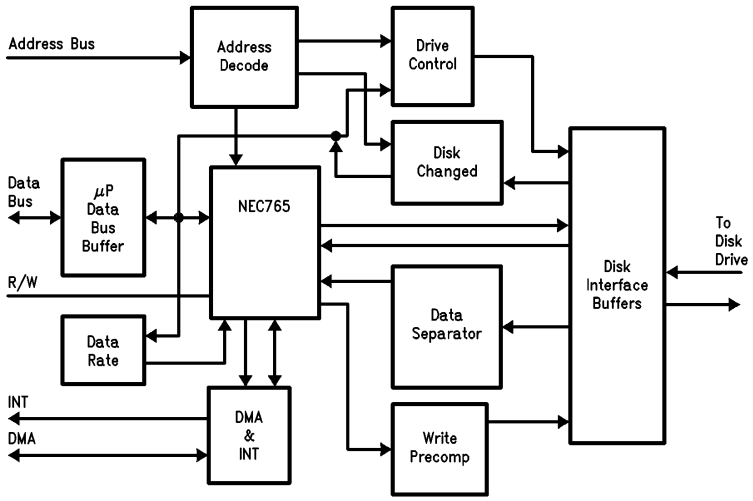

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FIGURE 11. Block Diagram of Floppy Controller Design with NEC765

DMA transfers must be slowed down due to handshaking problems with the NEC765A. This delay is performed with an external shift register.

This entire design easily requires at least a couple of dozen chips. The amount of board space used is quite large. A considerable amount of current is also consumed. The DP8473 solution only requires two chips. It is easy to see that the DP8473 solution is much more economical, and consumes less power and board space.

CONCLUSION

This design guide was created to answer the most common questions encountered while designing with the DP8473. Any new design can be based on the information given in this guide. A two drive system can be created or more drives can be added if required. A variety of disk drives may be used including 3.5″ drives.

The address decoding is the only function not integrated into the DP8473. However, the integrated data separator requires external filtering which should be carefully layed-out on the board.

If problems arise, there are many items that can be looked at to help identify where the problem exists. It may be useful to obtain a floppy controller diagnostic program similar to the ''Floppy Demo Program'' available from a National Semiconductor sales office.

If more information is desired concerning the performance of the data separator or the trade-offs of designing a custom filter for the PLL, please read the application note titled ''Floppy Disk Data Separator Design Guide for the DP8473'', AN-505.

Lit. # 100631

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